

# OBSAI RP3-01 6.144 Gbps Interface Implementation

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## Abstract

A cost-efficient digital hardware implementation for high speed RP3-01 serial interface at 6.144 Gbps is presented for an OBSAI compliant BTS systems. Such data rate represents a 8x increment of the lowest RP3-01 rate and it enables transmission of multiple wide-band carriers, to be used across multi-node RRH network infrastructures and across a wide range of wireless standards, including WiMAX 802.16e-2005 and 3GPP LTE wireless applications. The implementation is based on Altera EP2SGX90FF1508 FPGA device, which transceivers handles the electrical physical layer. The optical physical layer is implemented by Finisar SFP+ FTLX8571D3BCL devices. The upper layers of the RP3-01 protocol stack are implemented using Radiocomp's OBSAI RP3-01 IP core. This implementation is backward compatible with the existing RP3-01 line rates and the design methodology of the IP core makes it usable as well on lower cost FPGA families. The FPGA design flow used is based on Altera Quartus II 7.2 programming environment for simulations, synthesis and mapping into the target device. The system's performance is evaluated both with internal BER counters with PRBS-23 data representing valid RP3-01 traffic as well as with eye mask compliance using Agilent 86105 DCA for measurement.

**Keywords:** OBSAI, RP3, RP3-01, IP, 6.144 Gbps, Remote Radio Head, High Speed Interfaces, Radiocomp ApS, DTU, WiMAX, LTE, FPGA.

## INTRODUCTION

Open architectures have recently been introduced in wireless infrastructure networks for distributing and decentralizing Base Transceiver Stations (BTS). Such approaches aim mainly at reducing the relative capital (CAPEX), operating (OPEX), development expenditures and efforts while increasing system performances and flexibility by defining a modular and standardized interfaces and internal BTS architecture.

The BTS is an integral part of the radio access network and is the bridge between the handset and the wireless infrastructure core network. In a distributed BTS network architecture, the radio module is remote relative to the channel card (base-band processing) and communicates with the channel card via a standardized digital optical interface. Distance over the fiber vary from indoor coverage up to a few kilometers. This is done to improve site performances and reduce site footprint as well as enable high efficiency sector coverage with multiple remote radio nodes.

The Open Base Station Architecture Initiative (OBSAI) [1] defines a modular BTS architecture with standardized functions and inter-module interfaces (Fig.1).

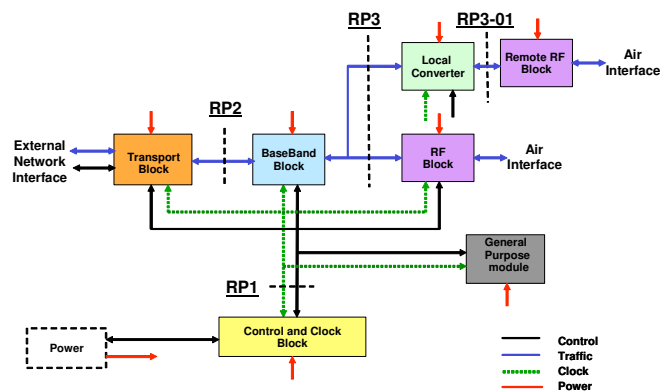


Figure 1: OBSAI Reference Architecture [11].

OBSAI defines the Remote RF Block or also called Remote Radio Head (RRH) concept as a radio module connected to the base-band through the Reference Point 3-01 (RP3-01) interface, as defined in [2]. The RP3-01 interface realizes a high speed optical communication link between the Local Converter (LC) module and the RRH. This interface is used to provide bi-directional transfer of digitized base-band radio data together with control and air-interface synchronization information [2].

Emerging wireless standards like WiMAX 802.16e-2005 [4] and 3GPP Long Term Evolution (LTE) [5] enhance throughput and radio signal quality performance also by defining wide-band radio channels in multi-carrier

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configurations and advanced modulation schemes for uplink and downlink channels.

The RP3-01 interface set the line rates up to 3.072 Gbps [1], which is a bottle-neck to provide wide-band carrier support in multi-node RRH setups. The impact that a 6.144 Gbps data rate increment will have on the existing RP3 standard specifications is regarding the identification of suitable technology standards for the physical layer including the definition of electrical specifications and optical transceiver modules, the logical and protocol design choices, and the evaluation of the system performances in terms of Bite Error Rate (BER) and limitations in terms of synchronization and timing.

The work described in this paper illustrates a suitable physical layer optical technology and the design choices required to demonstrate both electrical and optical 6.144 Gbps RP3-01 interface which requires minimal changes to the existing OBSAI RP3 definitions. The design is targeting an FPGA-based implementation usable for both BTS and RRH applications. The test setup consists of a full-duplex point-to-point electrical and optical communication at 6.144 Gbps between two Altera Stratix II GX Audio/Video (SIIGXAV) evaluation boards using coaxial cable pair for the electrical link and Enhanced Small Form-Factor pluggable (SFP+) transceiver for the optical link together with the RP3/RP3-01 IP engine (Fig.2).

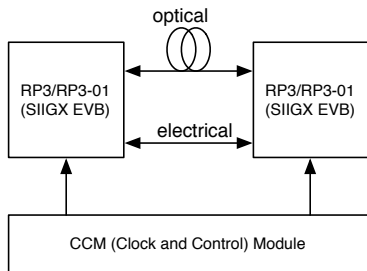


Figure 2: Test setup.

The RP3 bus clock signal [3] is provided externally while the RP3 frame synchronization reference is generated by internal 10-ms counters. The signal's quality is measured via internal Bit Error Rate (BER) counters in the design blocks and the signal eye diagram using Agilent 86105 equipment.

This paper is organized as follows: *Section II* outlines the bandwidth increment requirements for multi-node wide-band carriers RRH networks. *Section III* describes RP3-01 functional architecture and blocks. *Section IV* briefly describes the SFP+ transceiver technology benefits and shows measurements of the opti-

cal signal performances. *Section V* describes briefly the GX transceivers features shows measurements of their electrical performances. *Section VI* illustrates the RP3-01 design considerations for 6.144 Gbps and for low cost FPGA-based implementations. *Section VII* illustrates the hardware test setup and BER measurement results. The conclusions are given in *Section VIII*.

## II - BANDWIDTH REQUIREMENTS

In [4] a number of Orthogonal Frequency Division Multiple Access (OFDMA) profiles and radio channel bandwidths up to 28 MHz are defined in WiMAX [5]. 3GPP LTE [5] also supports a number of profiles and radio channels with bandwidths up to 20 MHz. Each channel bandwidth is associated with its base-band digital sample rate, where the samples are given in In-phase (I) and Quadrature (Q) format of 16 bits each or lower at the RP3-01 stage [2]. For such wireless standards, performance optimization and higher capacity on the radio link can be achieved by exploiting advanced Multiple-Input Multiple-Output (MIMO) antenna techniques<sup>1</sup> together with multi-carrier techniques, which are thus increasing the amount of antenna carriers required to be supported into a wireless site. Multiple sectors support and coverage optimization can be achieved by exploiting advanced configurations of multiple RRH nodes in a number of topologies, like daisy-chaining, ring or tree-and-branch.

The RP3-01 link has a limited support in terms of bandwidth available when it is required to transport multiple wide-band radio carriers signals across multiple RRH nodes using virtual RP3 links [2]. Tables 1 and 2 show an example of how many (X) wide-band carriers at 10 MHz and 20 MHz respectively can be transported over a 3.072 Gbps and over a 6.144 Gbps virtual RP3 links [2] respectively. In this case the whole RP3-01 link is allocated for a single air-standard standard and we assume that the RP3 virtual channel is specified by parameters (index,module) with value (0,1) and message mapping rules by making use of dual-bit map algorithm [2].

As an example of the advantages of a higher bandwidth provided from a 6.144 Gbps link applied to a common 802.16e-2005 WiMAX site setup, it is illustrated below in Fig.3 an optimized 3-sector OBSAI-based wireless site. Advanced RRH modules in Class 2 and Class 3 version [2] are depicted and a 6.144 Gbps RP3-01 link act as the main link to the BTS. Inter-RRH links can be used at a lower rate for cost reduc-

<sup>1</sup>MIMO technology offers significant increase in data throughput and wireless link range and robustness without requiring additional channel bandwidth or transmit power when compared to SISO (Single-Input Single-Output), giving as result thus a higher spectral efficiency and link reliability reducing fading.

Air-Interface	Sample Rate	Channel BW	X
802.16e	11.2 Msps	10 MHz	5
802.16e	22.4 Msps	20 MHz	2
LTE	15.36 Msps	10 MHz	4
LTE	30.72 Msps	20 MHz	2

Table 1: Maximum number of antenna carriers (X) that fit into a Virtual RP3/RP3-01 link at 3.072 Gbps.

Air-Interface	Sample Rate	Channel BW	X
802.16e	11.2 Msps	10 MHz	10
802.16e	22.4 Msps	20 MHz	5
LTE	15.36 Msps	10 MHz	8
LTE	30.72 Msps	20 MHz	4

Table 2: Maximum number of antenna carriers (X) that fit into a Virtual RP3/RP3-01 link at 6.144 Gbps.

tion of the optical transceiver technology (SFP+ vs. SFP). The setup has been accounting for a number of 2x2 MIMO RRH modules with OFDMA carriers each having 10 MHz channel bandwidth, and with the opportunity of extending capacity and dedicated coverage with additional RRHs (dashed lines in Fig.3).

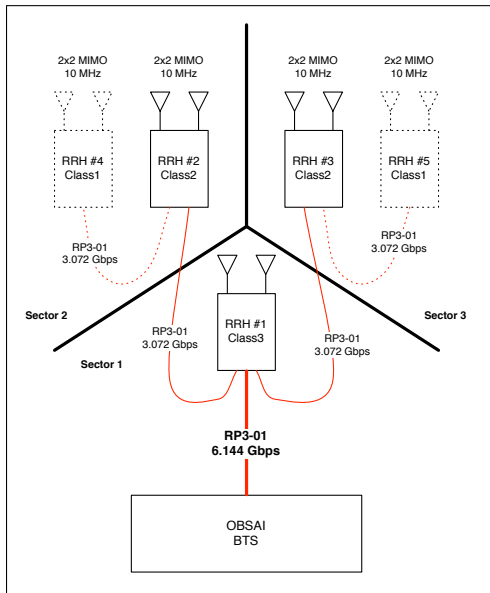


Figure 3: OBSAI RP3-01 6.144 Gbps based wireless site.

Based of these considerations, OBSAI RP3-01 line rate definitions up to 3.072 Gbps<sup>2</sup> are not providing the bandwidth required<sup>3</sup> to support a sufficient number

<sup>2</sup>Existing OBSAI RP3-01 rates are 768 Mbps, 1.536 Gbps and 3.072 Gbps.

<sup>3</sup>Mapping of WiMAX and LTE digitized radio samples into

of wide-band carriers across multiple sectors as shown in Table 1 while using a single fiber as main link between the site and the OBSAI BTS. The 6.144 Gbps line rate will double the RP3-01 link capacity and provide the necessary bandwidth for supporting advanced RRH network architectures for multi-sector coverage.

### III - IMPLEMENTATION ARCHITECTURE

The functional architecture of the RP3-01 interface design is represented in Fig.4, showing the split between the physical and the higher layers (Application, Transport, Data Link).

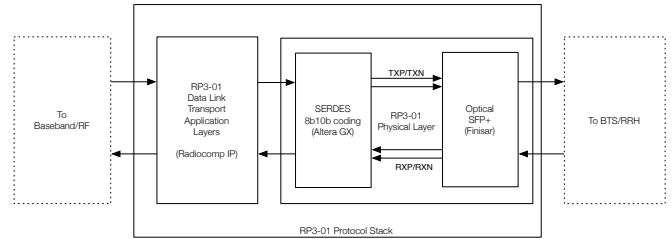


Figure 4: OBSAI RP3-01 6.144 Gbps architecture and data-path.

In this implementation the RP3-01 physical layer consists of high speed Stratix II GX transceivers and of optical SFP+ transceivers, while the logical layers are part of the Radiocomp's IP. The higher layer (Application) can be interfaced with Base-band or RF cards, while the lower layer (Data Link) is interfaced with the physical layer. The whole high speed design is hosted from the SIIGXAV evaluation board.

### IV - SFP+ OPTICAL TRANSCEIVER TECHNOLOGY

The SFP (Small Form-Factor Pluggable) compact optical transceivers are commonly used in optical communications for both telecommunication and data communication applications and they are Commercial-Off-The-Shelf (COTS) available devices with capability for data rates up to 4.25 Gbps. The latest generation of such transceivers, called Enhanced Small Form-Factor Pluggable (SFP+), have been designed within the same form-factor for higher data rates up to 10 Gbps, for lower power consumption, less complexity, and as a lower cost alternative to the 10-Gbps XFP form factor<sup>4</sup>. Fig.5 and Fig.6 are shown the eye diagram mea-

the OBSAI RP3-01 link is done using (index,module) and dual bit maps algorithm as defined in [2].

<sup>4</sup>10 Gigabit Small Form Factor Pluggable - Vendors in the cost-sensitive 10-Gigabit Ethernet (10 GbE) market are making a strong push to standardize SFP+ technology for use in 10 GbE

measurements of RP3-01 optical signals at 3.072 Gbps and 6.144 Gbps rates respectively on the SIIGXAV. The signal measured consist of valid RP3-01 frame structure<sup>5</sup> with data in every RP3-01 message slot. The measurements have been done using FTLX8571D3BCL 10Gbps 850nm Multimode Datacom SFP+ Transceiver. Optimized results may be achieved in the near future by using the FTLF8528P2BNV 8.5 Gbps Short-Wavelength SFP+ transceivers.

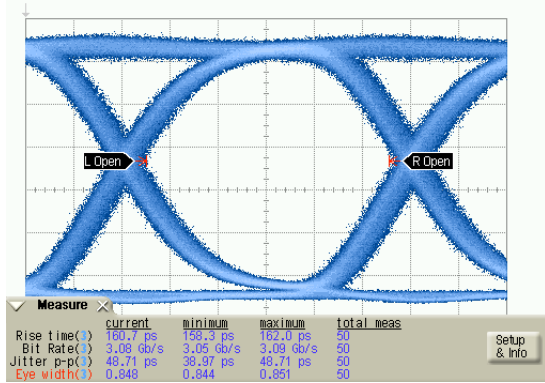


Figure 5: 3.072 Gbps RP3-01 optical signal.

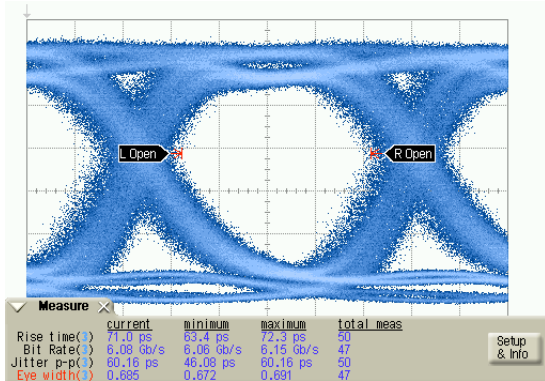


Figure 6: 6.144 Gbps RP3-01 optical.

These measurements are taken using Agilent 89105 DSO equipment over 1m distance with multimode 850 nm fiber. The instrument has been configured with a 153.6 MHz trigger reference locked to the transmitted data, which consist of valid RP3-01 data messages. At 3.072 Gbps rate a 3.125 Gbps rate filter is applied. At 6.144 Gbps a 9.125 Gbps rate filter is applied, since the 6.250 Gbps filter option was not available for measuring.

In [2] the values for eye mask compliance relative to the eye width for OBSAI RP3 transmitter / receiver are 0.65 Unit Interval (UI) / 0.45 UI respectively using 3.072 Gbps rates and they are 0.7 UI / 0.4 UI using 6.144 Gbps rates. The eye diagram measurement at

applications and similar as an alternative to the XFP form factor.

<sup>5</sup>Which includes frame boundary marking characters (K28.7) and Message Group boundary marking characters (K28.5).

3.072 Gbps rate shows a peak-to-peak jitter value at 48.71 ps with a eye width value at 0.848 UI. The eye diagram measurement at 6.144 Gbps rate shows a peak-to-peak jitter value at 60.16 ps with a eye width value at 0.685 UI. Both these measurements show mask compliance of the OBSAI RP3/RP3-01 transmitted and received signal.

## V - HIGH SPEED SERDES TECHNOLOGY

The physical electrical layer is implemented by the Altera Stratix II GX device family, which combines up to 20 duplex channels capable of operating between 600 Mbps and 6.375 Gbps into a single FPGA. The low power transceivers offer appropriate signal integrity and provide a number of features such as Dynamic Pre-emphasis, Equalization and Adaptive Equalization. The transceivers also provide appropriate jitter performance, meaning they comply electrically with the majority of serial standards being used today, including many of the telecom standards. For OBSAI RP3/RP3-01 applications, they offer compliance to the XAUI electrical interface specified in Clause 47 of IEEE 802.3ae-2002 [10] up to 3.072 Gbps and to the Common Electrical I/O (CEI) for both the Short Reach and Long Reach 6.25 Gbps standards (CEI-6G-SR and CIE-6G-LR) [6], which is a suitable standard recommendations for applications above 3.072 Gbps.

The GXB transceiver includes dedicated blocks to support a number physical layer functionalities of many key protocols built inside the transceiver. In the case of OBSAI RP3/RP3-01, the 8b10b encoding and word alignment blocks and synchronization/phase alignment buffers are embedded in the transceiver block and do not need to use dedicated FPGA logic.

The relevant GXB transceiver configuration used is as it follows in Table 3:

GXB Configuration Parameter	Value
double data mode	true
data rate	6144
protocol	6G basic
equalizer	0
pre-emphasis	0
8b10b enc/dec	cascaded
ref clk	153.6 MHz
rx cru pll	tx clk

Table 3: GB Transceiver configuration

Also dynamical reconfiguration of each transceiver from one operating mode to another is supported. This mode reconfiguration involves reconfiguring of the data

rate, data path, or both [7]. For this implementation a fixed double-width data-path of 32-bits is chosen and only data rate settings are set being dynamically reconfigurable from the user<sup>6</sup>.

Fig.7 and Fig.8 shows the eye diagram measurements of 3.072 Gbps and 6.144 Gbps electrical signals respectively on the SIIGXAV<sup>7</sup>. The signal measured consist of valid RP3-01 frame structure<sup>8</sup> with data in every RP3-01 message slot.

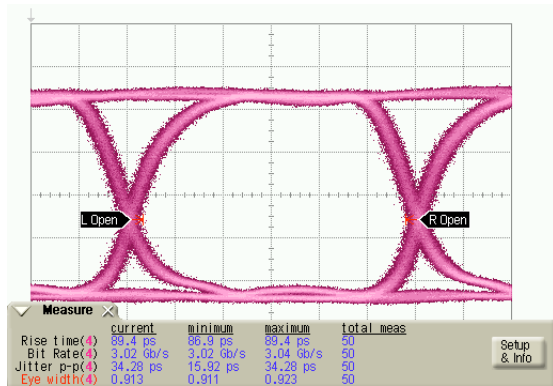


Figure 7: 3.072 Gbps RP3-01 electrical signal.

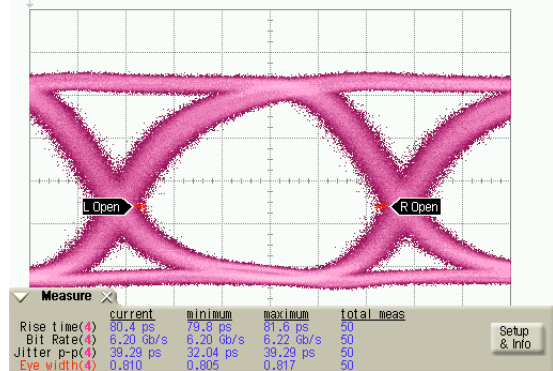


Figure 8: 6.144 Gbps RP3-01 electrical signal.

These measurements are taken using Agilent 89105 DSO equipment that has been configured with a 153.6 MHz trigger reference synchronized to the transmitted data, which consist of valid RP3-01 data messages.

In [2] the values for eye mask compliance relative to the eye width for OBSAI RP3 transmitter / receiver are 0.65 UI / 0.45 UI respectively using 3.072 Gbps rates and they are 0.7 UI / 0.4 UI using 6.144 Gbps rates. The eye diagram measurement at electrical 3.072 Gbps

<sup>6</sup>In case of dynamic reconfiguration enabled in double-width mode, only the 768 Mbps line rate is not supported from the transceivers since only line rates between 1 Gbps and 6.25 Gbps are allowed.

<sup>7</sup>These measurements are performed with the standard analog pre-emphasis and equalization settings on the ALT2GX8 Megawizard.

<sup>8</sup>Which includes frame boundary marking characters (K28.7) and Message Group boundary marking characters (K28.5).

rate shows a peak-to-peak jitter value at 34.28 ps with a eye width value of 0.913 UI.

The eye diagram measurement at electrical 6.144 Gbps rate shows a peak-to-peak jitter value at 39.29 ps with a eye width value at 0.810 UI.

Both these measurements show mask compliance of the OBSAI RP3/RP3-01 transmitted and received signal.

## VI - RP3-01 TIMING AND CONFIGURATION

The OBSAI BTS has a reference system clock (SCLK) of 30.72 MHz provided externally compliant with the requirements as specified in [3]. This is used as a convenient frequency for operations at a value eight times multiple of the WCDMA chip rate<sup>9</sup>. The RP3-01 interface reference frequency is different from SCLK, since an overhead of 3 bytes per RP3 message and additional control bandwidth are defined in [2], and the next convenient way if getting this extra bandwidth is a higher frequency reference multiple of 12.5 ( $\times 10/8$ ) times the SCLK, thus 38.4 MHz. The RP3-01 byte clock frequency is a multiple of 38.4 MHz and it is defined being a factor of 10 the line rate used due to the 8b10b coding and phase locked to SCLK [2]. Table 4 illustrates the core clock frequencies according to the data path chosen.

Rate (Mbps)	8DP clk (MHz)	32DP clk (MHz)
6144	614.4	153.6
3072	307.2	76.8
1536	153.6	38.4
768	76.8	19.2

Table 4: OBSAI RP3-01 core clock frequencies for 8-bits and 32-bits data paths respectively.

To design with lower cost FPGA technology while maintaining the same serial throughput, higher data-path parallelization is chosen to lower the operating core clock frequency. In this design 6.144 Gbps and 32 bits data-path are chosen, giving a 153.6 MHz frequency.

This operating frequency enables usage of the RP3-01 IP block also in low-cost Altera Cyclone II and Cyclone III families, which internal logic supports maximum operating frequencies of around 167 MHz [8] and around 180 MHz [9] respectively. In this case an external physical layer SERDES technology it is required.

The RP3-01 frame structure parameters are defined in [2] and reported in Table 5, and they are the same for WCDMA, WiMAX and LTE configurations.  $i$  defines the frame structure according to the line rate used, and it takes integer values according to Table 6. In this implementation value eighth ( $i=8$ ) is chosen. Thus only

<sup>9</sup>The WCDMA chip rate is 3.84 Mcps.

reconfiguration of  $i$  parameter and of the core clock frequency is required to enable dynamic line rate re-configuration from the RP3-01 IP core.

M_MG	N_MG	K_MG	i
21	1920	1	variable

Table 5: RP3-01 Frame structure for WCDMA, 802.16 and LTE.

Line Rate (Mbps)	i
768	1
1536	2
3072	4
6144	8

Table 6: Line rate and “i” parameter values definition.

## VII - TEST SETUP AND RESULTS

The test setup block architecture is illustrated in Fig.9 where two SIIGXAV boards are connected to implement a full duplex optical communication at 6.144 Gbps of valid RP3-01 traffic. The measurements was also performed at 3.072 Gbps for comparing the 6.144 Gbps line rate results to the existing RP3 specifications Setup options for the RP3-01 IP and GX transceivers are done via DIP switches. External clock generator is used to generate 153.6 MHz for both the boards and the trigger signal to the 89105 DSO.

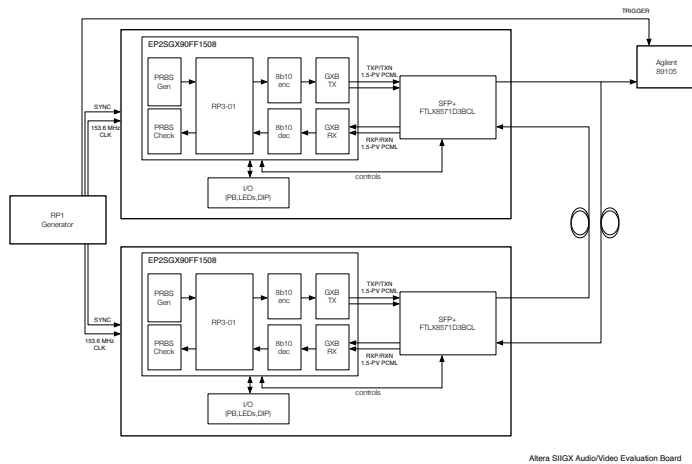


Figure 9: Block diagram of the test setup.

The Pseudo Random Bit Sequence (PRBS) generator blocks implements a simple 3-bytes counter for the RP3-01 message header and a 16-bytes counter for the RP3-01 message payload for each message slot<sup>10</sup> in a

<sup>10</sup>RP3/RP3-01 message slot size is defined as 19 bytes [2].

Message Group. A PRBS validator checks the received messages counters values and the BER counter measures the amount of bit errors received. The system setup is given in Fig.10, where the 7-segments display on each board shows the BER counter values and the LED bank shows that the system is correctly operating according to the mapping in Table 7.

LED	Signal	High	Low
1	TX PLL	unlocked	locked
2	RX PLL	unlocked	locked
3	RP3-01 RX IDLE	false	true
4	RP3-01 RX SYNC	false	true
5	PRBS Errors	present	not present
6	LCV Errors	present	not present
7	RE-SYNC	on	off
8	not used	-	-

Table 7: Status LED mapping.



Figure 10: Hardware setup.

The results indicate that the transmission at 6.144

Gbps over each link is error free (zero value is monitored constantly on both receivers) and measured over a time window of a few days and without using any additional bit-level scrambling layer between data link layer and 8b10b coding blocks. It has been possible to verify the correct operational status of the interface through the LED bank status indication that are mapped as indicated in Table 6 and they all show “low” logic values as expected.

## VIII - CONCLUSIONS

A 6.144 Gbps OBSAI RP3-01 point-to-point full-duplex transmission test setup was built running at 153.6 MHz bus clock. Radiocomp’s OBSAI RP3-01 IP is supporting all OBSAI RP3-01 line rates including the 6.144 Gbps extension via a parameter configuration only. Stratix II GX dynamic channel reconfiguration also is supporting multiple rate configurations and backward compatibility with 3.072 Gbps link have been demonstrated using SFP+ FTLX8571D3BCL optical transceivers as RP3-01 physical layer. The measurements of the signal integrity compare the 3.072 Gbps with the 6.144 Gbps eye diagram with acceptable signal’s eye quality, proving an error-free communication with internal BER measurements.

## ACKNOWLEDGMENTS

Thanks to Radiocomp ApS for permission of using their RP3-01 IP core for this implementation. Thanks to Altera for providing evaluation boards and software tools and valuable discussions. Thanks to Finisar and Laser2000 for providing SFP+ FTLX8571D3BCL samples. Thanks to Agilent for providing the 86100 measurement equipment.

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## TRADEMARKS

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